ABSTRACT

The invention uses a standard processor to execute an application program. As the instructions of the application program are executed in sequence, a program counter is incremented to contain an address indicator of the next instruction to be executed. The address indicator from the program counter is also fed to a function lookup unit where it is matched to the contents of a tag field. If there is no match, control returns to the processor which continues its normal sequence of operations and performs the function. If there is a match, function indicator identifiers from the function lookup table are fed to a reconfigurable combinational array which has logic functions. The function indicator identifiers select the logic function to be performed. The result of the performed function including the new program counter is then fed back to the processor. The processor then continues its normal operations.